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Architectural Strategies of Low Power VLSI Versatile Multimedia Functional Unit

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***Abstract* - Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major consideration, where power dissipation has become as important a consideration as performance and area. This paper reviews various strategies and methodologies for designing low power circuits and systems. It describes the many issues facing designers at architectural, logic, circuit and device levels and presents some of the techniques that have been proposed to overcome these difficulties. The paper concludes with the future challenges that must be met to design low power, high performance systems. In the past, the major concerns of the VLSI designer were area, performance, cost and reliability; power consideration was mostly of only secondary importance. In this paper we introduced the low power VLSI techniques in the architecture of VMFU. In this paper we implemented radix 4 algorithm and SPST technique in VMFU. The VMFU is a multiplexer controlled system. Multiple operations can be achieved by changing the selection bits of multiplexer. Approximately 30% of power can be reduced by using these low power VLSI techniques. The power estimation can be analysed with X-Power Analyser of XILINX tool and multiple operations can be simulated by using MODELSIM software.**

***Keywords* - Versatile Multimedia Functional Unit (VMFU), Radix- 4 Booth Algorithm, Spurious Power Suppression Technique (SPST), Multiplexer.**

I. INTRODUCTION

Power dissipation is recognized as a critical parameter in modern VLSI design field. To satisfy MOORE'S law and to produce consumer electronics goods with more backup and less weight, low power VLSI design is necessary. Dynamic power dissipation which is the major part of total power dissipation is due to the charging and discharging capacitance in the circuit. The golden formula for calculation of dynamic power dissipation is Pd = CLV2f. Power reduction can be achieved by various manners. They are reduction of output Capacitance CL, reduction of power supply voltage V, reduction of switching activity and clock frequency f. In this section we introduced the above three technologies to encounter the unnecessary power dissipation problems Hybrid CSA[1] is mostly adopted in Multiplier circuits. Modified Booth Encoding is adopted in Multipler and VMFU. Transient power minimization Method is applicable for Multipler, VMFU and ETD(H.264)[5].In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Several factors have contributed to this trend. Perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices (portable desktops, audio- and video-based multimedia products) and wireless communications systems (personal digital assistants and personal communicators) which demand high-speed computation and complex functionality with low power consumption. In these applications, average power consumption is a critical design concern. The projected power budget for a battery-powered, A4 format, portable multimedia terminal. The basic idea is that, instead of shifting and adding for every column of the multiplier term and multiplying by 1 or 0, we only take every second column, and multiply by ±1, ±2, or 0, to obtain the same results. The advantage of this method is the halving of the number of partial products [4]. To Booth recode the multiplier term, we consider the bits in blocks of three, such that each block overlaps the previous block by one bit. Grouping starts from the LSB, and the first block only uses two bits of the multiplier. Figure 1 shows the grouping of bits from the multiplier term for use in modified booth encoding. The below diagram shows process of Radix-4 Booth Encoding method, which reduces number of partial products [10].

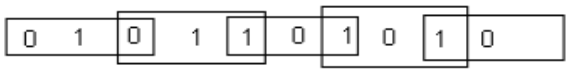

Fig.1. Radix-4 Booth Grouping

Each block is decoded to generate the correct partial product. The encoding of the multiplier Y, using the modified booth algorithm, generates the following five signed digits, -2, -1, 0, +1, +2. Each encoded digit in the multiplier performs a certain operation on the multiplicand, X, as illustrated in Table

Block	Re - coded digit	Operation on X
000	0	0 X
001	+1	+1 X
010	+1	+1 X
011	+2	+2 X
100	-2	-2 X
101	-1	-1 X
110	-1	-1 X
111	0	0 X

Comparing the MSP for different cases

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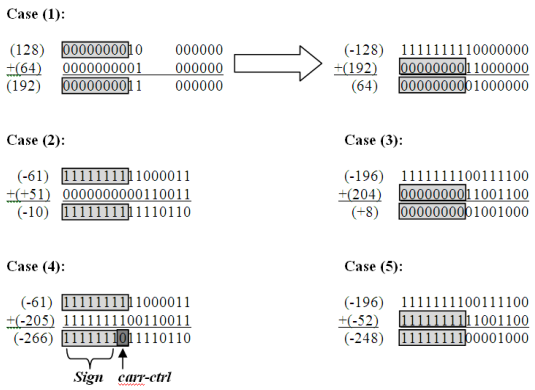

Fig.2. Process of Suppression of MSP

As shown in the above Fig.2 The total power is divided in to MSB POWER and LSB POWER. By using Transient Power minimization technique we can eliminate MSB POWER, Provided Msb data should not Affect the computation[2]. In the Above Figure .The 1st case illustrates a transient state in which the spurious transitions of carry signals occur in the MSP though the final result of the MSP are unchanged. The 2nd and the 3rd cases describe the situations of one negative operand adding another positive operand without and with carry from LSP, respectively. Moreover, the 4th and the 5th cases respectively demonstrate the addition of two negative operands without and with carry-in from LSP. In those cases, the results of the MSP are predictable Therefore the computations in the MSP are useless and can be neglected. The data are separated into the Most Significant Part (MSP) and the Least significant Part (LSP). To know whether the MSP affects the computation results or not. We need a detection logic unit to detect the effective ranges of the inputs. The Boolean logical equations shown below express the behavioral principles of the detection logic unit in the MSP circuits of the SPST-based adder/subtractor: The Detection Unit Decides Whether MSB is Allowed or Eliminated. By using this technique we can Suppress Power up to 22%.

Block diagram of VMFU-Based on the selection values the VMFU performs six operations this method consist of three stages [2],[7].

- Partial product generation
- Partial product reduction
- Accumulation process

➢ If the selection bits are 100 the operation is SAD(successive Approximation Division)
➢ If the selection bits are 000 the operation is Addition
➢ If the selection bits are 010 the operation is Subtraction
➢ If the selection bits are 110 the operation is Interpolation
➢ If the selection bits are 001 the operation is Multiplication
➢ If the selection bits are 111 the operation is MAC

In this paper three techniques are implemented in VMFU to suppress the power and to increase the speed. Booth encoding and SPST techniques finds more applications in DSP and Multimedia Applications.

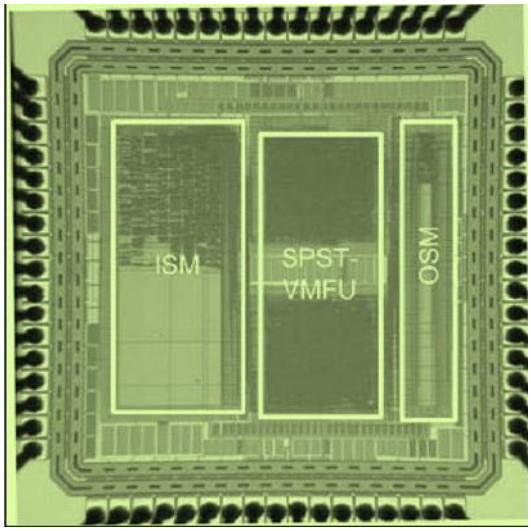

Fig.3. Chip micrograph of VMFU

Principle of power suppression

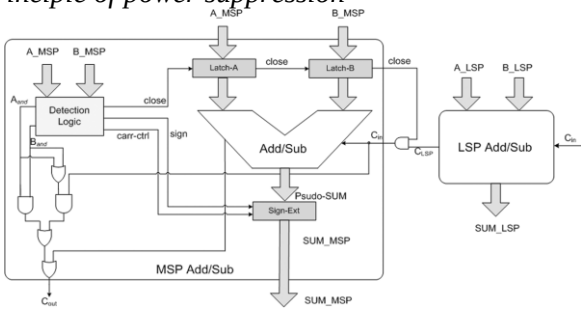

Fig.4. Block Diagram of SPST

Above Figure shows a 16-bit adder/subtractor design example adopting the proposed SPST. In this example, the 16-bit adder/subtractor is divided into MSP and LSP between the eighth and the ninth bits. Latches implemented by simple AND gates are used to control the input data of the MSP. When the MSP is necessary, the input data of MSP remain unchanged. However, when the MSP is negligible, the input data of the MSP become zeros to avoid glitching power consumption. The two operands of the MSP enter the detection-logic unit, except the adder/subtractor, so that the detection-logic unit can decide whether to turn off the MSP or not. Based on the derived Boolean equations (1) to (8), the detection-logic unit of SPST is shown which can determine whether the input data of MSP should be latched or not. Moreover, we propose the novel glitch-diminishing technique by adding three 1-bit registers to control the assertion of the *close*, *sign*, and *carr-ctrl* signals to further decrease the transient signals occurred in the cascaded circuits which are usually adopted in VLSI architectures designed for multimedia/DSP applications. A certain amount of delay is used to assert the *close*, *sign*, and *carr-ctrl* signals after the period of data transition which is achieved by controlling the three 1-bit registers at the outputs of the detection-logic unit.[5].

Hence, the transients of the detection-logic unit can be filtered out; thus, the data latches shown in Fig can prevent the glitch signals from flowing into the MSP with tiny

cost. The data transient time and the earliest required time of all the inputs are also illustrated. The delay should be set in the range of, which is shown as the shadow area in Fig, to filter out the glitch signals as well as to keep the computation results correct[6].

HDL code for Top module

```
moduleTOP_SPST(clock,rst,X,Y,sel,VMFU_OUT);
    parameter Addition        = 3'b000;
    parameter Multiplication  = 3'b001;
    parameter Subtraction     = 3'b010;
    parameter SAD             = 3'b100;
    parameter Interpolation   = 3'b110;
    parameter MAC             = 3'b111;
    input clock,rst;
    input signed [15:0]X,Y;
    input [2:0]sel;
    output reg [33:0]VMFU_OUT;
    reg [33:0] INTRPLTN;
    wire [33:0] SAD_OUT;
    wire [31:0]MULTIPLICATION;
    wire [33:0]SUB_OUT,MAC_OUT;
    wire [33:0]ADD_OUT;
    wire [31:0]MULT_OUT;
     reg [31:0]acc;
     always @ (posedge clock)
     begin
      if (rst)
     begin
      VMFU_OUT = 34'b0;
      acc      = 34'b0;
      INTRPLTN = 34'b0;
      end
      else
      begin
      case (sel)
         3'b000 : begin
                  VMFU_OUT = ADD_OUT;
                  end
       3'b001 : begin
                  VMFU_OUT = MULT_OUT;
                  end
    3'b010 : begin
                  VMFU_OUT = SUB_OUT;
                  end
   3'b100 : begin
                  VMFU_OUT = SAD_OUT;
                  end
 3'b110 : begin
                  INTRPLTN = (X + Y)>> 1;
                  VMFU_OUT = INTRPLTN;
                  end
3'b111 : begin
                  acc = acc + MULT_OUT;
                  VMFU_OUT = acc;
                  end
        default : begin
                  VMFU_OUT = 34'b0;
      end
      endcase
      end
      end
Carry_Sv_ADDCSA(.a1(X),.a2(Y),.sum(ADD_OUT));MU
LTIPLIERMULT
(.clock(clock),.Multiplier(X),.Multiplicand(Y),.Final_OUT
_reg(MULT_OUT));
    TOP_MACMAC1
(.clock(clock),.rst(rst),.X(X),.Y(Y),.MULTIPLICATION(M
ULTIPLICATION),.Final_out(MAC_OUT));
    SUB  SUB1 (.X(X),.Y(Y),.D(SUB_OUT));
    SAD  SAD1 (.X(X),.Y(Y),.SAD_OUT(SAD_OUT));
  endmodule
```

Analysis of Detection Process

1) When the detection-logic unit turns off the MSP At this moment, the outputs of the MSP are directly compensated by the SE unit; therefore, the time saved from skipping the computations in the MSP circuits shall cancel out the delay caused by the detection-logic unit.*2) When the detection-logic unit turns on the MSP* The MSP circuits must wait for the notification of the detection-logic unit to turn on the data latches to let the data in. Hence, the delay caused by the detection-logic unit will contribute to the delay of the whole combinationalcircuitry, i.e., the16-bit adder/subtractor in this design example.*3)When the detection-logic unit remains its decision* No matter whether the last decision is turning on or turning off the MSP, the delay of the detection logic is negligible because the path of the combinational circuitry (i.e., the 16-bit adder/subtractor in this design example) remains the same.[4]

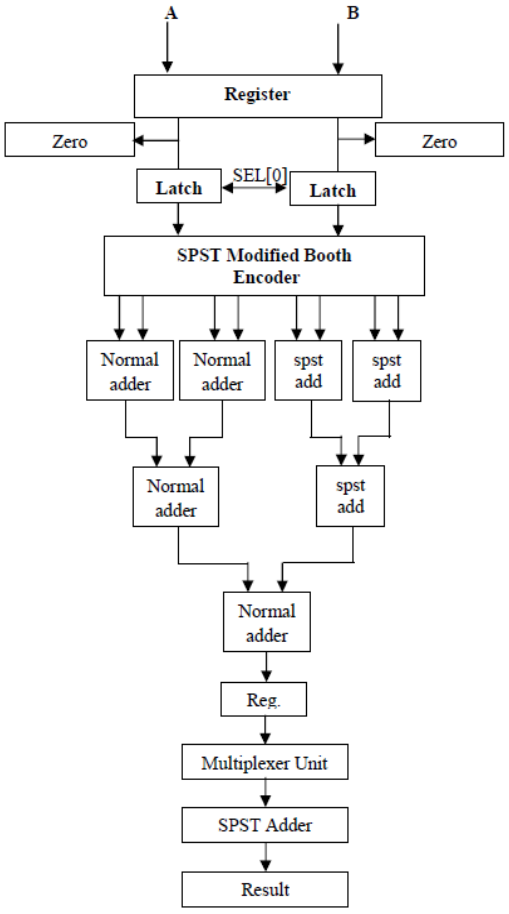

Fig.5. Block Diagram of VMFU

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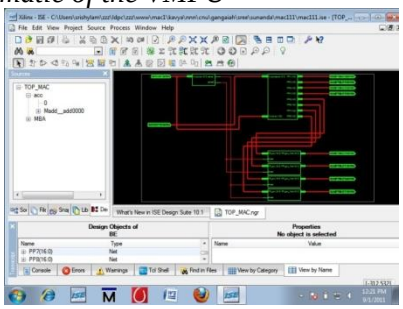
II. Result and Analysis

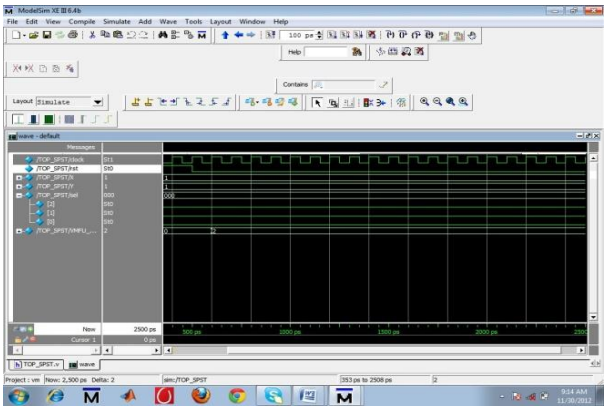
By using VMFU we can obtain SIX oparations with low power .The multiplexer is incorporated in this VMFU. Modelsim is used to simulate the SIX oparations. In this paper all simulation results shown(six). XILINX is used to Synthesise the verilog code. This work involves 25 verilog modules. X-power analyser of XILINX is use3d to anlyse the power.

RTL Schematic of the VMFU

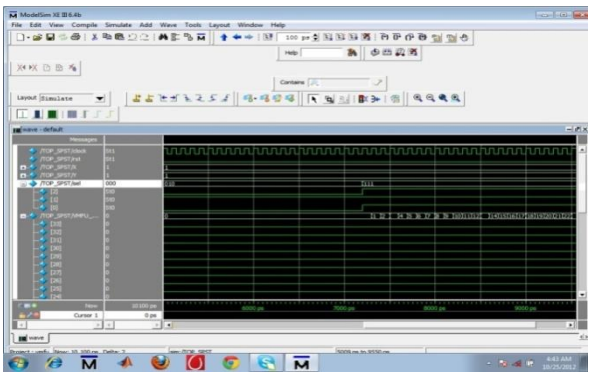


III. Simulation Screenshots

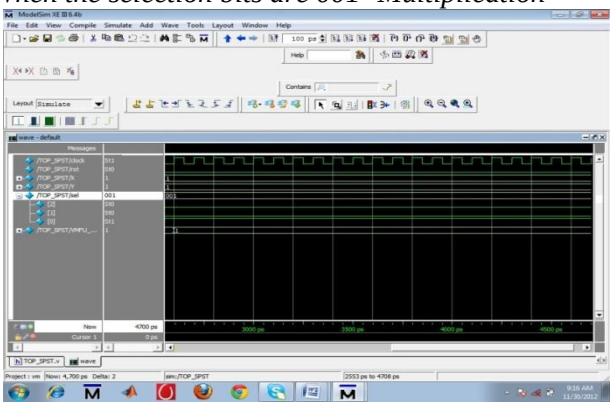
Selection bits are 000 –Addition



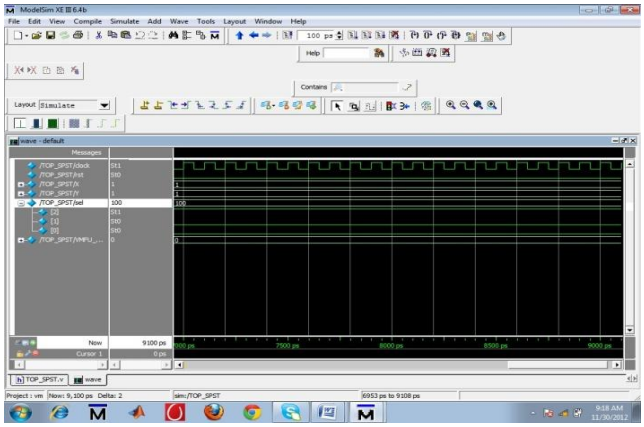
Selection bits are 010- Subtraction



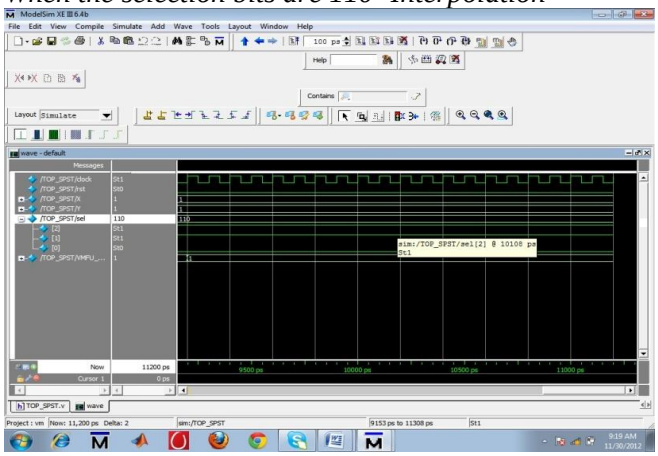
When the selection bits are 001- Multiplication



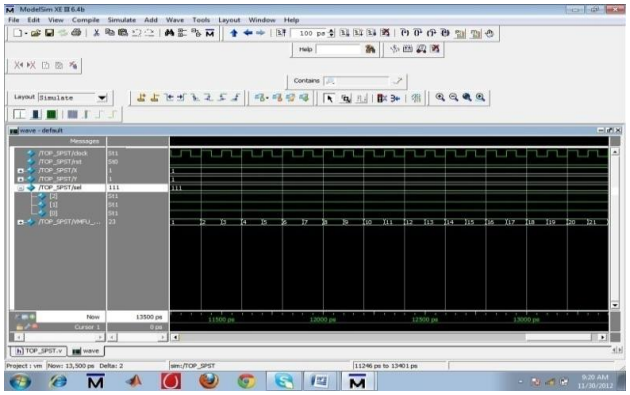
When the selection bits are -100 SAD



When the selection bits are 110- Interpolation



When the selection bits are 111 MAC



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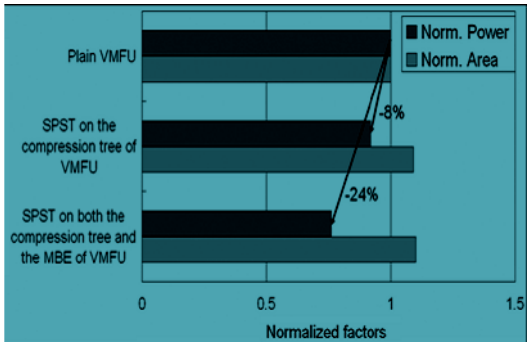
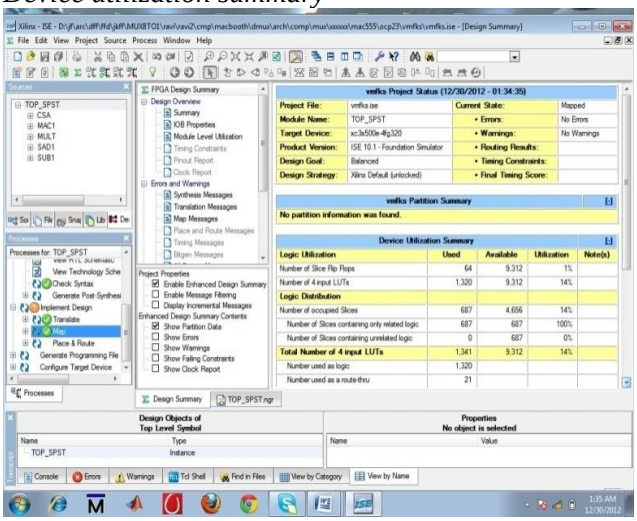
The below diagram shows power reduction analysis.If we observe the Normalized power ,it is reduced 0% without VMFU(plain vmfu).In second case -8% power is reduced with SPST and VMFU.In third case -24% i.e24% is reduced with SPST,Booth algorithm(mbe) and Vmfu Technologies.

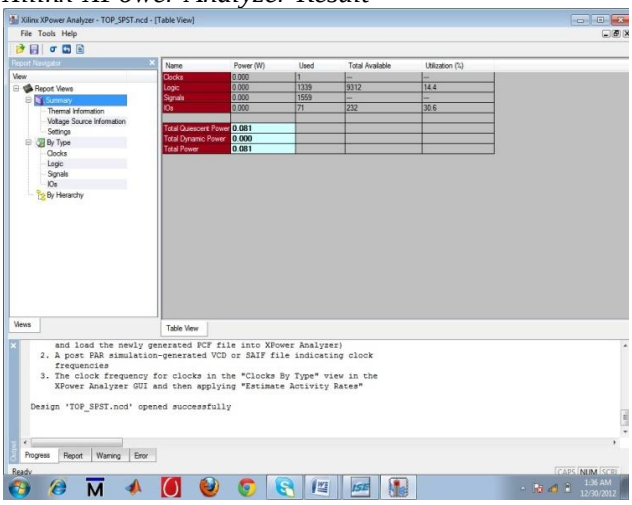
In this paper Two VLSI Tools are used. To Synthesise the VERILOG CODE,XILINX is used and MODELSIM is used to simulate the code.We achieved the SIX operations without any errors.The code also dumped on to the FPGA kit.



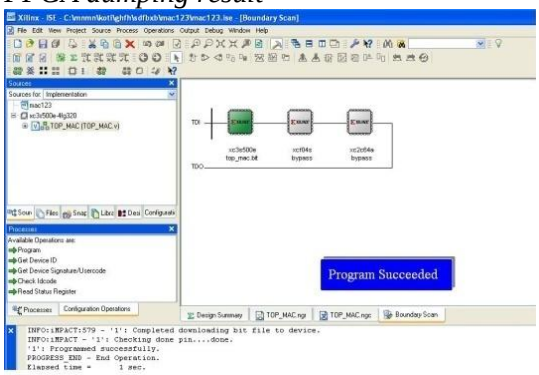
Device utilization summary



Xilinx-XPower Analyzer Result



FPGA dumping result



IV. Conclusion and Future Scope

In this paper, we discussed the implementation of modified booth algorithm, hybrid CSA and transient minimization power techniques for the design unit VMFU. By using modified booth encoding technique we can increase the speed of the system and by using Power transient minimization method we can reduce the power up to 24%. By combining CSA and accumulation process we can form a hybrid CSA, which is the most suitable application of multiplier.

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